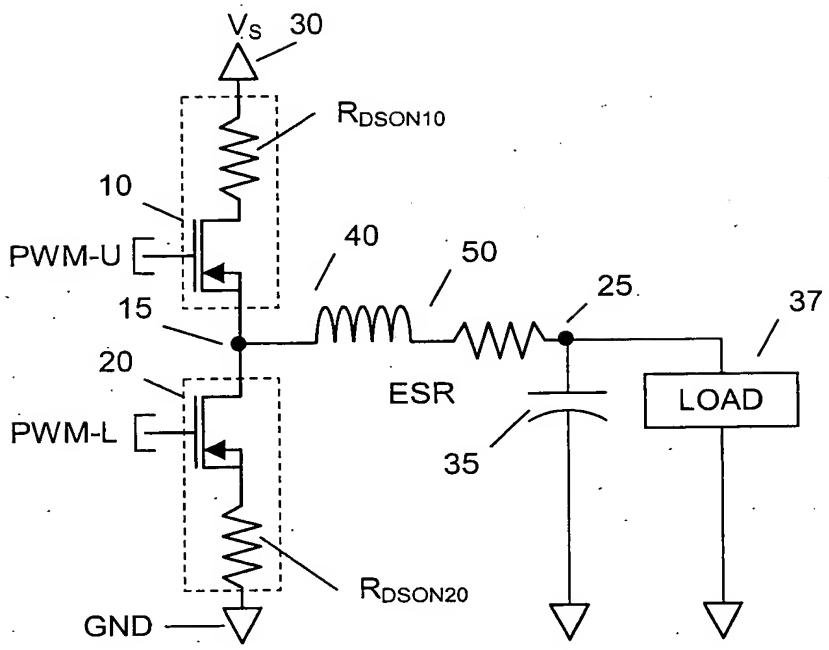


FIG 1
(Prior Art)

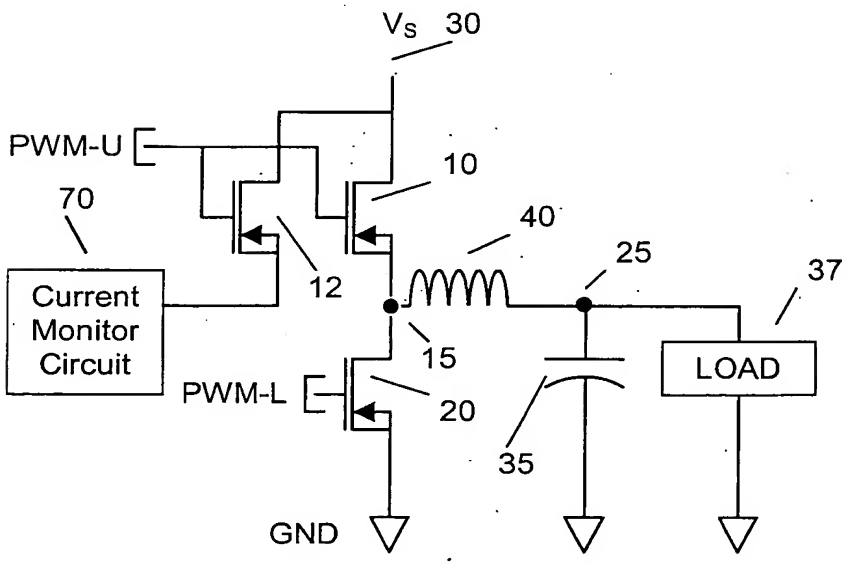


FIG 2
(Prior Art)

FIG 3
(Prior Art)

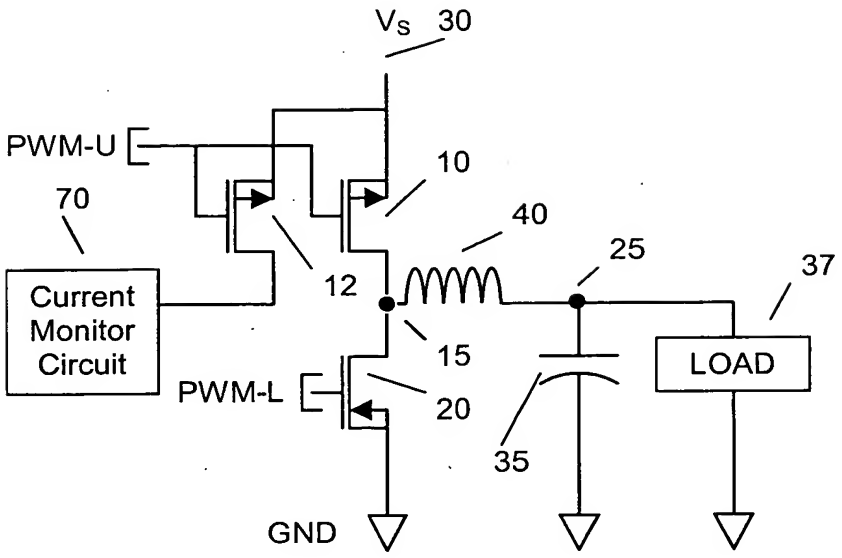


FIG 4

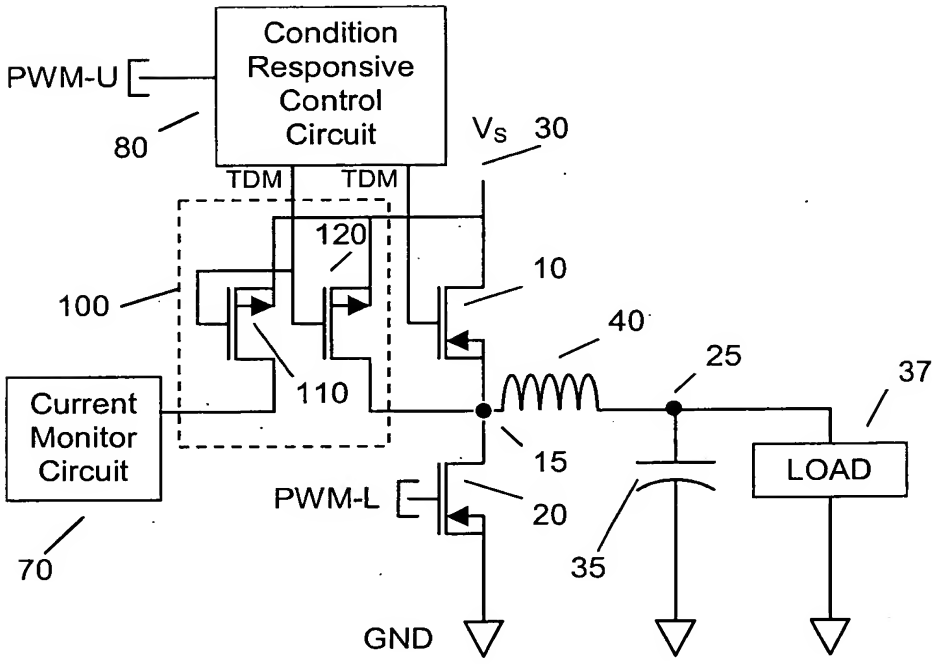


FIG 5

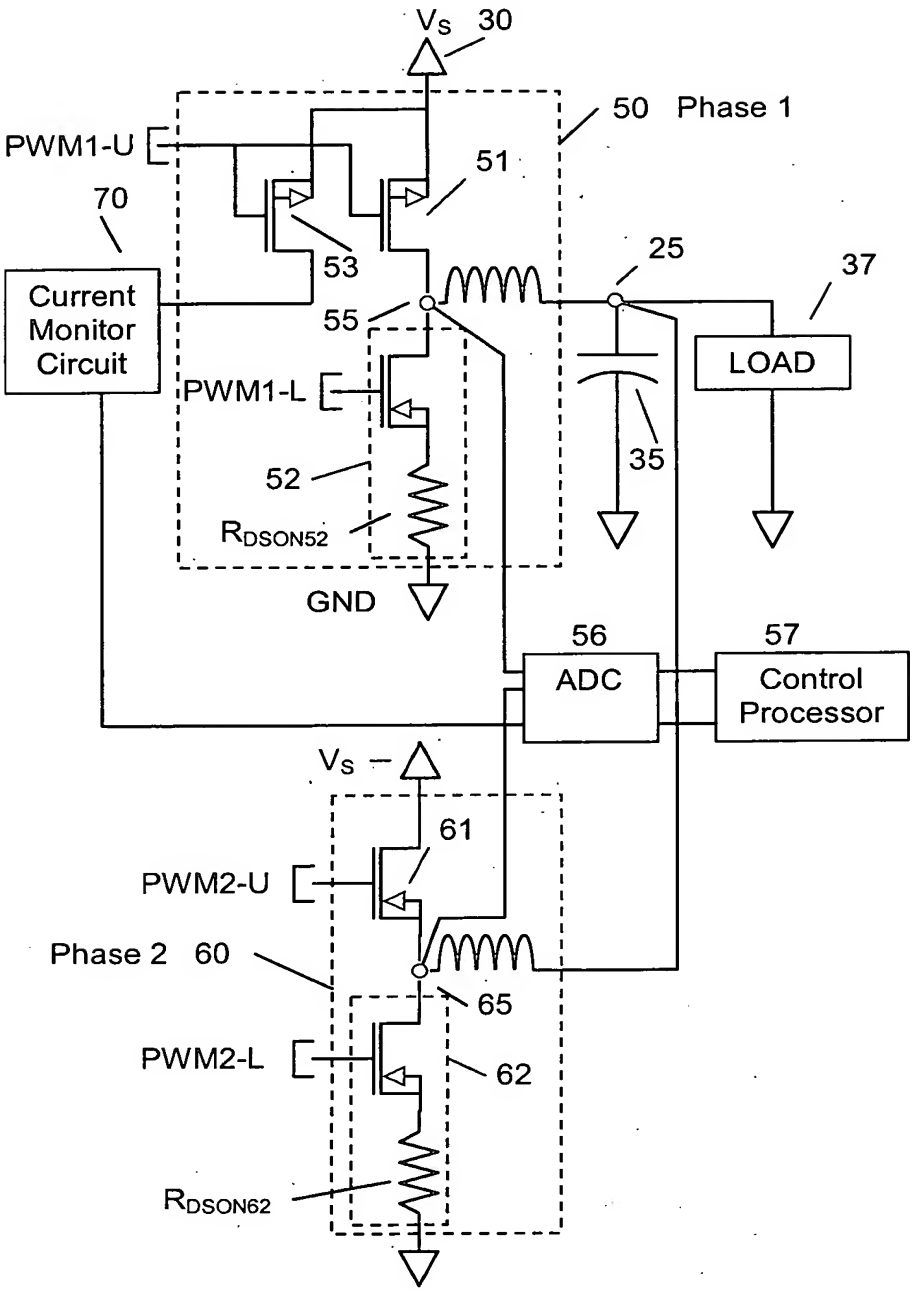
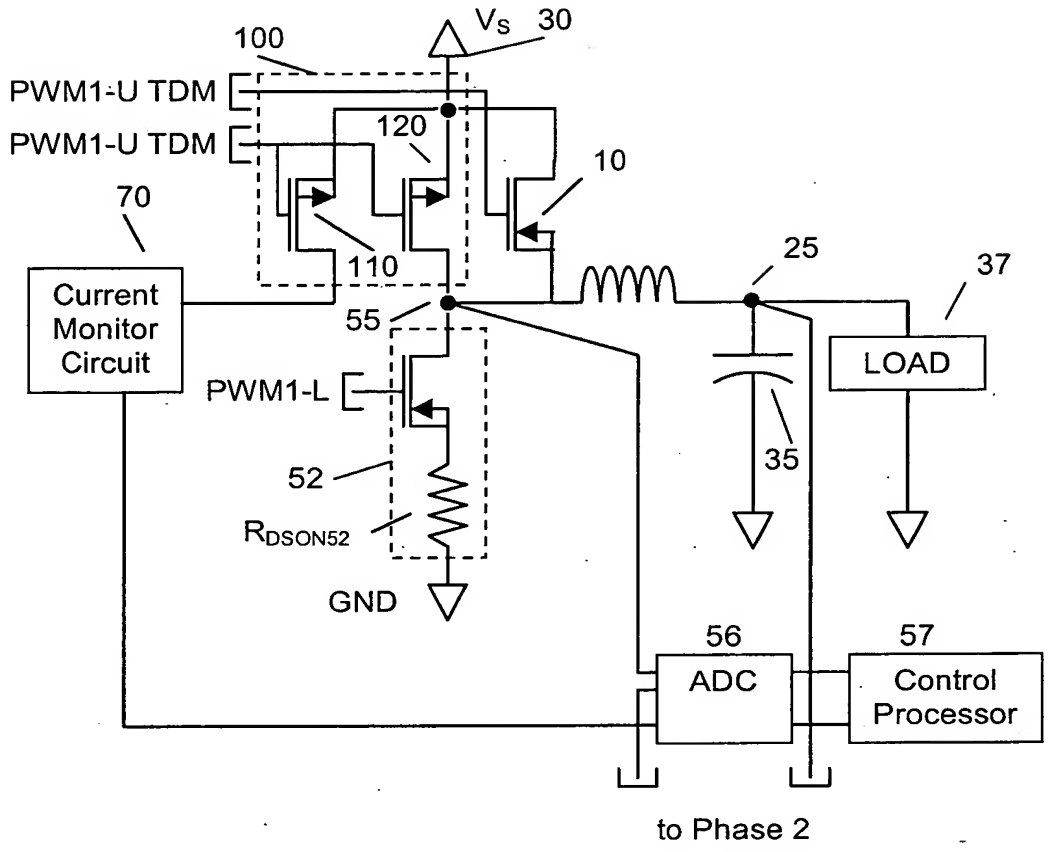

V_S 30
50 Phase 1
PWM1-U
51
70
53
25
37
Current Monitor Circuit
55
LOAD
PWM1-L
35
52
R_{DSON52}
GND
56
57
ADC
Control Processor
V_S
61
PWM2-U
Phase 2 60
65
PWM2-L
62
R_{DSON62}

FIG 6


100
V_S 30
PWM1-U TDM
PWM1-U TDM
120
10
70
110
25
37
Current Monitor Circuit
55
LOAD
PWM1-L
35
52
R_{DSON52}
GND
56
57
ADC
Control Processor
to Phase 2